FIG. 1

FIG. 2

START

PLACE PROCESSOR CORE IN TEST MODE — 21

GENERATE ONE OR MORE PSEUDO-RANDOM/DETERMINISTIC TEST VECTORS FOR PERIPHERAL DEVICES USING MISSION DATA PATHS OF PROCESSOR CORE, PROVIDE THE TEST VICTORS TO SCAN CHAINS, RECOVER PRE-TEST STATE OF SCAN CHAINS OR TEST RESPONSES TO THE PRIOR SET OF TEST VECTORS AND COMPACTING THE TEST RESPONSES AS THEY ARE RECOVERED — 22

APPLY TEST VECTORS TO PERIPHERAL DEVICES, STORING TEST RESPONSES INTO SCAN CHAINS — 23

DONE ? — 24

NO

YES

RESTORE SAVED STATE OF SCAN CHAINS, RECOVER TEST RESPONSES TO LAST SET OF TEST VECTORS, COMPACTING TEST RESPONSES AS THEY ARE RECOVERED — 25
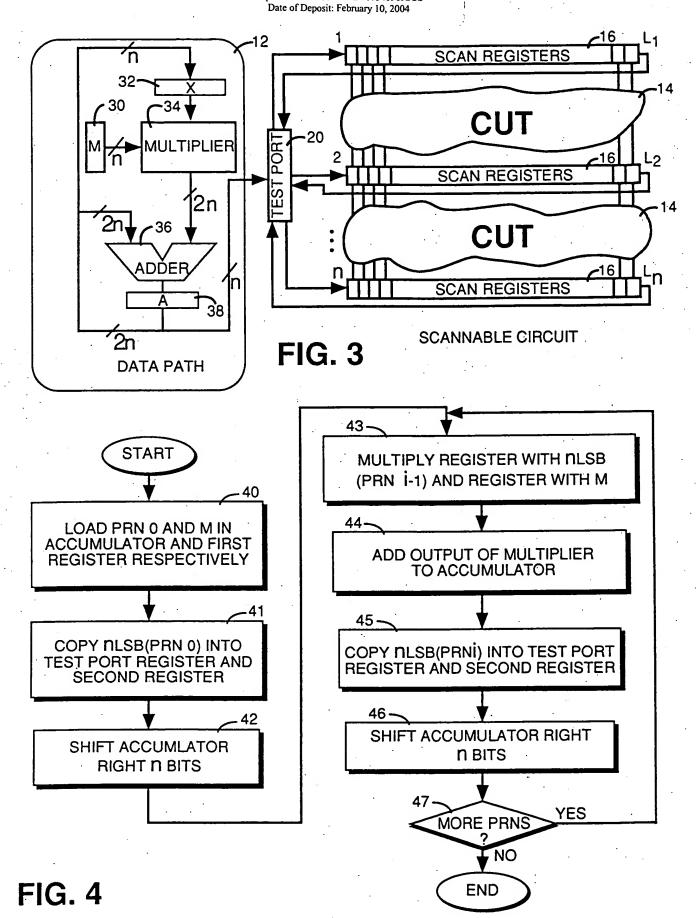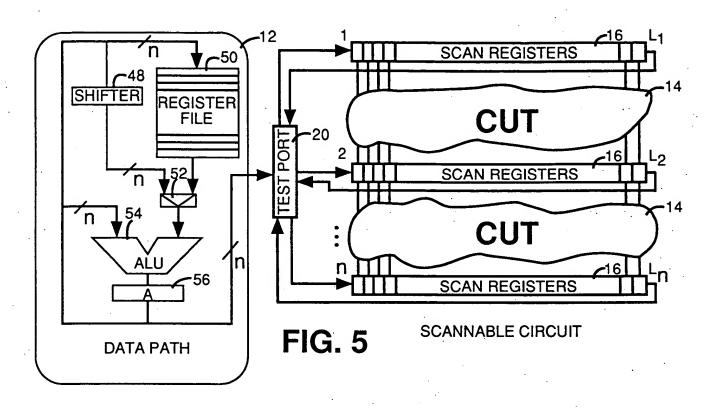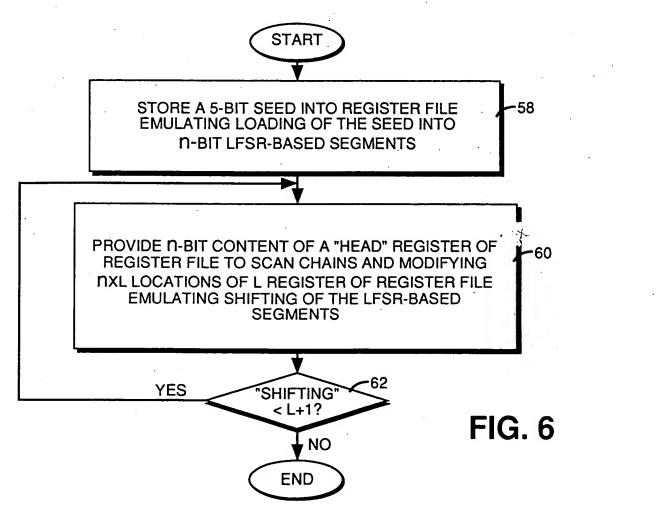
END

Justin D. Wagner
Our Ref. No.: 1011-67625
For: ARITHMETIC BUILT-IN SELF TEST OF MULTIPLE
SCAN-BASED INTEGRATED CIRCUITS
Inventor(s): Rajski et al.
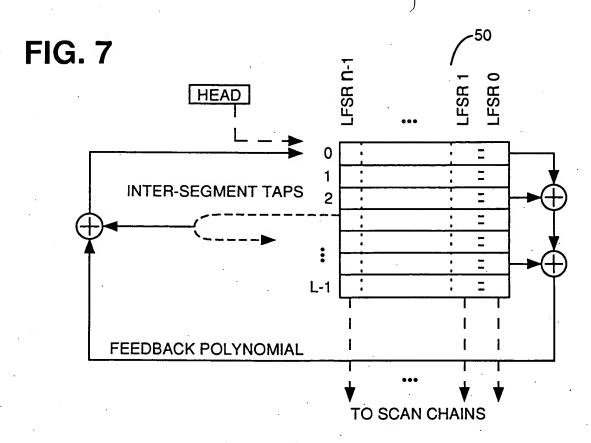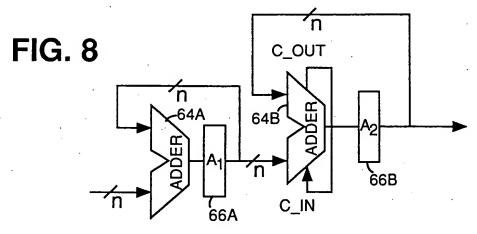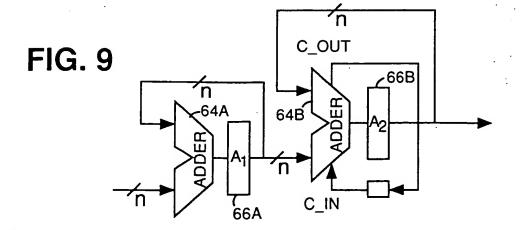Express Mail Label No. EV175409692US
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FIG. 3

DATA PATH

SCANNABLE CIRCUIT

FIG. 4

START

LOAD PRN 0 AND M IN ACCUMULATOR AND FIRST REGISTER RESPECTIVELY — 40

COPY nLSB(PRN 0) INTO TEST PORT REGISTER AND SECOND REGISTER — 41

SHIFT ACCUMLATOR RIGHT n BITS — 42

MULTIPLY REGISTER WITH nLSB (PRN i-1) AND REGISTER WITH M — 43

ADD OUTPUT OF MULTIPLIER TO ACCUMULATOR — 44

COPY nLSB(PRNi) INTO TEST PORT REGISTER AND SECOND REGISTER — 45

SHIFT ACCUMULATOR RIGHT n BITS — 46

MORE PRNS ? — 47   YES

NO

END

FIG. 5

DATA PATH

SCANNABLE CIRCUIT

START

STORE A 5-BIT SEED INTO REGISTER FILE
EMULATING LOADING OF THE SEED INTO
n-BIT LFSR-BASED SEGMENTS — 58

PROVIDE n-BIT CONTENT OF A "HEAD" REGISTER OF
REGISTER FILE TO SCAN CHAINS AND MODIFYING
$n \times l$ LOCATIONS OF L REGISTER OF REGISTER FILE
EMULATING SHIFTING OF THE LFSR-BASED
SEGMENTS — 60
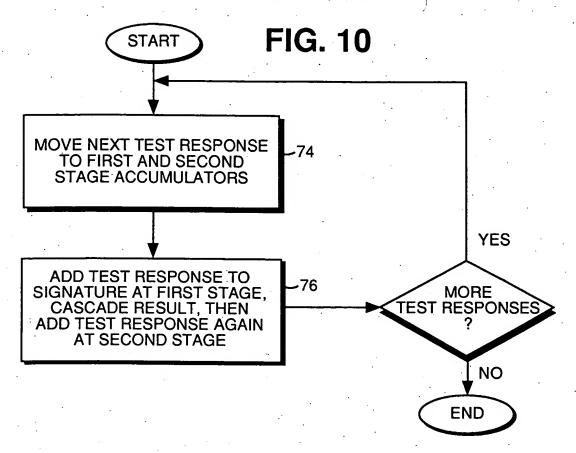
YES   "SHIFTING"
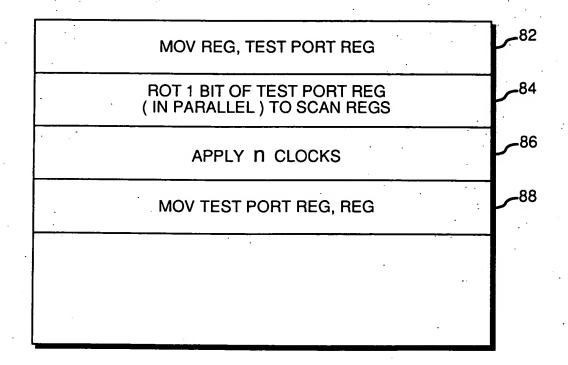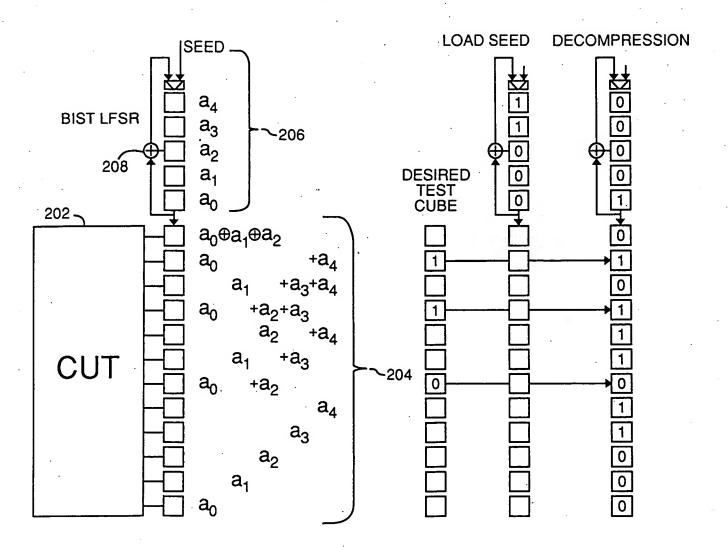< L+1?   — 62

NO

END

FIG. 6

Justin D. Wagner
Our Ref. No.: 1011-67625
For: ARITHMETIC BUILT-IN SELF TEST OF MULTIPLE
SCAN-BASED INTEGRATED CIRCUITS
Inventor(s): Rajski et al.
Express Mail Label No. EV175409692US
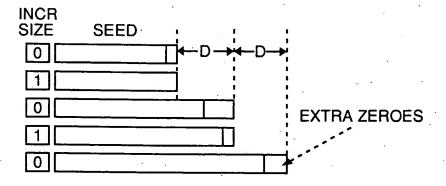Date of Deposit: February 10, 2004

FIG. 7

FIG. 8

FIG. 9

FIG. 10

START

MOVE NEXT TEST RESPONSE
TO FIRST AND SECOND
STAGE ACCUMULATORS — 74

ADD TEST RESPONSE TO
SIGNATURE AT FIRST STAGE,
CASCADE RESULT, THEN
ADD TEST RESPONSE AGAIN
AT SECOND STAGE — 76

MORE
TEST RESPONSES
?

YES

NO

END

FIG. 11

MOV REG, TEST PORT REG	82
ROT 1 BIT OF TEST PORT REG (IN PARALLEL) TO SCAN REGS	84
APPLY n CLOCKS	86
MOV TEST PORT REG, REG	88

FIG. 12

FIG. 13

FIG. 14